Appendix: Preliminary Capital Costs and Manpower for GASPARD

We have based our very preliminary cost estimates on a system with 15 000 detection channels.

A. Si and Calorimeter Detectors and Mechanics

We base our estimation on a conception of DSSD followed by thick padded Silicon detector and a gamma detector based on CsI scintillators:

Item	Costs in k€
DSSD & Si padded detectors	700
CsI and PM or avalanche PD	500
Mechanics	500
Total	1,700

The costs and manpower for R&D for the Si modules are estimated to be 140 k€ and 12 FTE, respectively. The costs and manpower for R&D for the CsI modules are estimated to be 60 k€ and 4 FTE, respectively. These estimates include the costs and manpower to build a demonstrator that will cover 1/15 of the active area of GASPARD. We assume that engineering, design and construction as well as characterization and final detector mounting and cabling will be performed using existing infrastructure. We expect an additional 10 % increase of the costs in case spare modules are required. The FTE includes the simulation tasks.

Total development costs: 200 k€
Total material costs: 1,700 k€
Total Manpower requirements : 16 FTE

B. Front End Electronics and Data Acquisition

The electronics and DAQ for the array has to handle both the Si recoil array and the surrounding calorimeter array for gamma and particle detection. These detector systems have a total of approximately 15 000 channels. The electronics comprises of two ASIC for Si readout (handling DSSD and PIN diodes) with at least 32 channels/chip. The cost assumes 32 channels/chip and any greater integration will produce some savings. The ASICs will be mounted with the pre-amp chips close to the detectors. The signal handling chip will be on cards which contain 10 ASICs (320 channels) multiplexed into a single output to an ADC card for readout. The multiplexer will use look-at-me logic to identify active channels rather than scanning all possible inputs. The ADC cards will have 8 inputs, each multiplexed down from 320 channels, so that each card handles 2560 channels, and 8 such cards will be needed in the full version. ADC cards will also contain an FPGA (Field Programmable Gate Array) and Ethernet readout (currently the best candidate is the Xilinx Virtex 4FX family of FPGAs with built in Ethernet MAC). The Gbit Ethernet fibre data links will transfer data through network switches to the DAQ system (PC farm). Mass storage is provided by the DAQ, as is a globally synchronised

timestamp system. All data words will be time-stamped using a time distribution system. Software triggers will be built in the DAQ's processor farm. Other front end electronics for any smaller subsystems (e.g. neutron arrays, magnetic spectrometers) will be interfaced to the DAQ using an interface card which timestamps the data using the same time distribution system. This mechanism allows conventional triggered data to be merged with the free running time-stamped data from parts of the system which will use software triggering. In this way the array will have a coherently integrated, but not uniform, system of front end electronics and DAQ.

B.1.1 ASIC capital cost:

Considering an ASIC with 32 channels of preamp, shaper, discriminator, sampler, TAC and multiplexer, then for 15 000 channels we require 480 ASICs.
Consider 500 chips/wafer (100 mm^2 each) then we need 1 wafer – buy 2 for spares. Assume that the packaging cost is €50 each chip and calculate cost for packaging all 3 wafers.

Submission before final production	60 k€
Mask set:	55 k €
3 wafers:	15 k €
Packaging:	75 k €
Total for 1500 ASICs:	**205 k €**

B.1.2 ASIC board capital cost:

Assume 10 chips/board plus some passive components and one intelligent chip (DSP or FPGA). Then we need 48 boards (60 including 12 spares). The NRE is split across 60 units: 5000/60 € ~ 85 € per board.

Components (except ASICs) 250 €
PCB cost 150 €
NRE costs (1/60 share) 85 €
Assembly cost 150 €
Total unit price 635 €
Price for 60 units = 38 100 k€

B.1.3 ADC board capital cost:

Assume that we bring ASIC signals from 1 ASIC board into a single ADC and that we mount 8 ADCs per ADC card then we need 8 ADC cards for 60 ASIC cards (includes spares). The NRE is split across 8 units: 5000/8 € ~ 625 € per board. Include one intelligent chip (FPGA) in each board to interface via XPORT to Ethernet, for control and Gbit Ethernet for readout)

Components 300 €
PCB cost 150 €
NRE costs (1/8 share) 625 €
Assembly cost 150 €
Total unit price 1225 €

Price for 8 units = 9 800 k€

B.1.4 Total Capital cost for array FEE:

ASIC: 1,500 units at a total cost of	205 000 k€
ASIC board: 60 units at total cost of	38 100 k€
ADC board: 8 units at a total cost of	9 800 k€
3 racks with 7 crates and power	40 000 k€
HT and detector power units	120 000 k€
Total capital costs for electronics:	**412 900 k€**

B.1.5 Manpower:

Manufacturing will be undertaken in industry, not in labs so all manufacturing manpower is included in capital costs. Some low level of manpower is needed for supervising the contracts and liaising with manufacturers. This is less than **1 FTE**.

B.2 Development costs for array FEE:

B.2.1 ASIC prototypes:

Assume that we need 2 prototype iterations of a 100sq mm chip on AMS 0.35u process then the cost of each iteration is about 60,000 €. So ASIC development cost is 120 k€

B.2.2 Electronics prototypes:

ADC and ASIC cards: one off using costs listed above with full NRE: approx 6k € per card for ADC and ASIC card: 12 k €.

B.2.3 R&D Manpower:

B.2.3.1 ASIC Manpower:

Assume that we use 2 engineers full time for 3 years: 6 FTE.

B.2.3.2 Other Electronics Manpower:

Assume that we use 2 engineers full time for 1 year to make the ASIC and ADC boards: 2FTE

Assume that we use 1 engineer (hardware or maybe software) full time for 1 year to program the intelligent devices (FPGAs) on the ADC and ASIC boards: 1FTE.

B.2.3.3 Software Manpower:

Assume that we use 2 people for 1 year to program the slow control and the GUI: 2FTE.

Total Manpower for development (R&D) 11 FTE

B.2.3.4 Total development cost:

ASIC development	120 k€
Electronics prototype	12 k€
Total Development	**132 k€**

Manpower **11 FTE**

C. Summary of capital costs and manpower for GASPARD.

	Costs k€	**Manpower FTE**
R&D Phase		
Detectors PA & GA (appendix A)	**200**	**16**
Front End Electronics (appendix B.2)	**132**	**11**
Construction Phase		
Detector (appendix A)	**1,700**	*****
FEE and acquisition (appendix B.1)	**413**	**1**
TOTAL	**2,445**	**28***

** Not yet fully defined.*